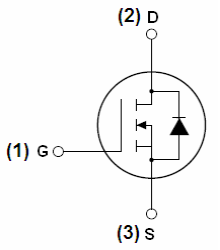
General Features

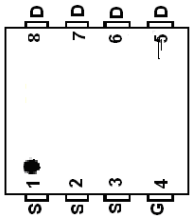
VDSS	RDS(ON) @10V (typ)	RDS(ON) @4.5V (typ)	ID
60V	6.8 mΩ	9.5 mΩ	45A

- Split Gate Trench Power MV MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Optimized for fast-switching applications
- RoHS Compliant

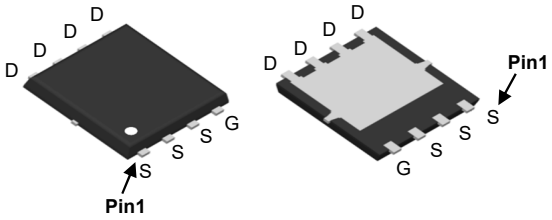
Applications

- Synchronus Rectification in DC/DC and AC/DC Converters
- Industrial and Motor Drive applications





Top View



DFN 3x3-8L

Ordering Information

Part Number	Marking	Case	Packaging
GT45N06	GT45N06	DFN3*3-8L	3000pcs/Reel

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current G	T_A=25°C	I_D	45	A
	T_A=100°C		25	
Pulsed Drain Current C		I_{DM}	80	A
Avalanche energy L=0.5mH C		E_{AS}	180	mJ
Power Dissipation A	T_A=25°C	P_{DSM}	50	W
	T_A=100°C		20	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Maximum		Units
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	18	22	°C/W
Maximum Junction-to-Ambient A D	Steady-State		55	72	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.1	2.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	60	65		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.1	1.7	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		6.8	8.2	mΩ
		V_{GS}=4.5V, I_D=20A		9.5	12.0	mΩ
g_{FS}	Diode Forward Voltage	V_{DS}=5V, I_D=20A	30			S
V_{SD}	Diode Forward Voltage	I_S=20A,V_{GS}=0V		0.85	0.99	V
I_S	Maximum Body-Diode Continuous Current [G]				53	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		1988		pF
C_{oss}	Output Capacitance			470		pF
C_{rss}	Reverse Transfer Capacitance			14		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.6		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=20A		31		nC
Q_g(4.5V)	Total Gate Charge			16		nC
Q_{gs}	Gate Source Charge			6		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-on Delay Time	V_{GS}=10V, V_{DS}=15V, R_L=2.5Ω, R_{GEN}=3Ω		10.5		ns
t_r	Turn-on Rise Time			4.5		ns
$t_{D(off)}$	Turn-off Delay Time			29.5		ns
t_f	Turn-off Fall Time			8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A,di/dt=500A/μs		17		ns
Q_{rr}	Body Diode Reverse Recovery charge	I_F=20A,di/dt=500A/μs		58		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature TJ(MAX)=150° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

Typical Performance Characteristics

Fig 1: Output Characteristics

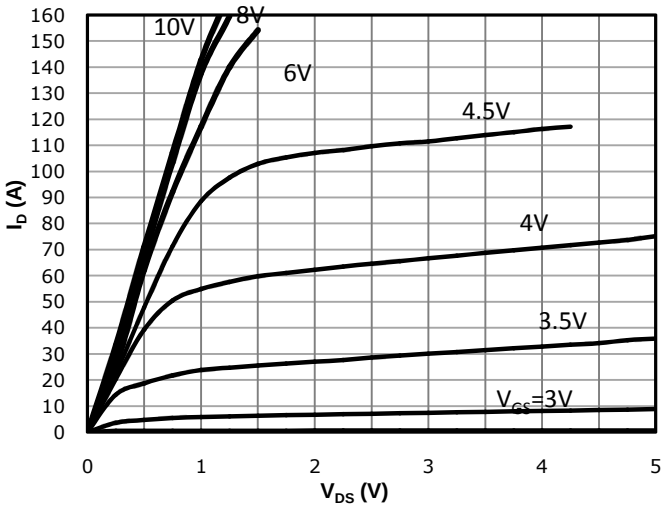


Fig 2: Transfer Characteristics

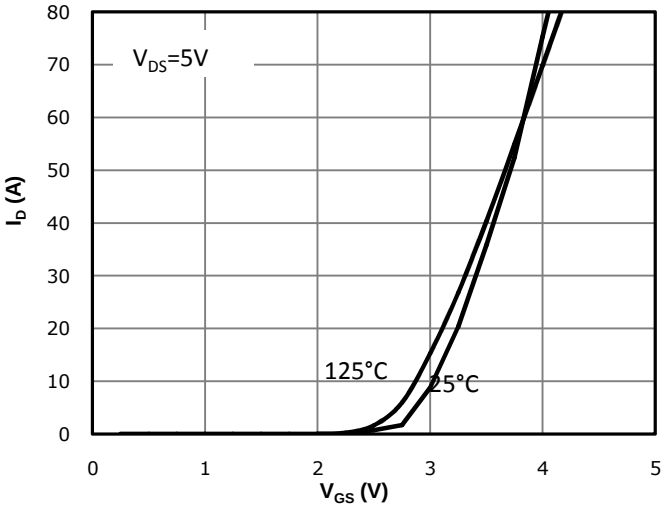


Fig 3: Rds(on) vs Drain Current and Gate Voltage

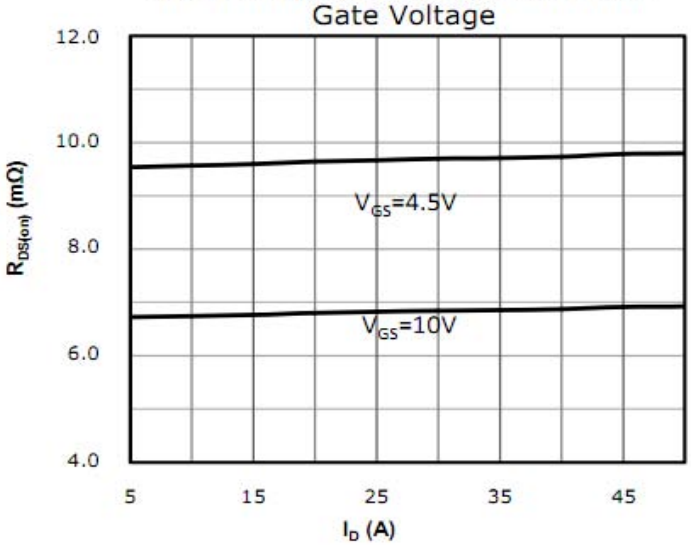


Fig 4: Rds(on) vs Gate Voltage

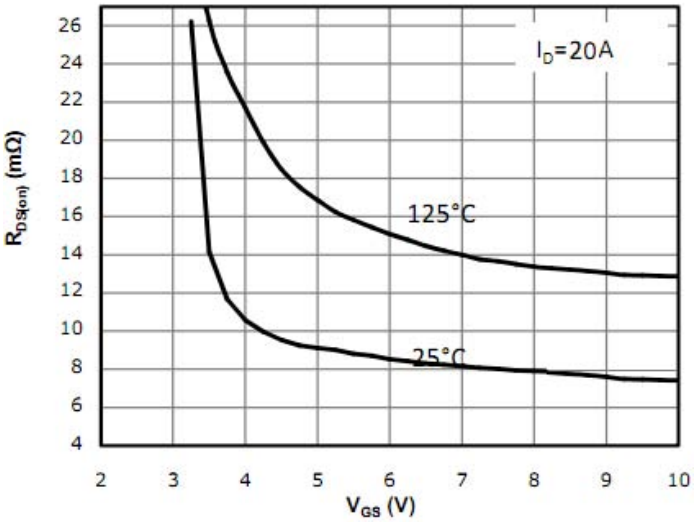


Fig 5: Rds(on) vs. Temperature

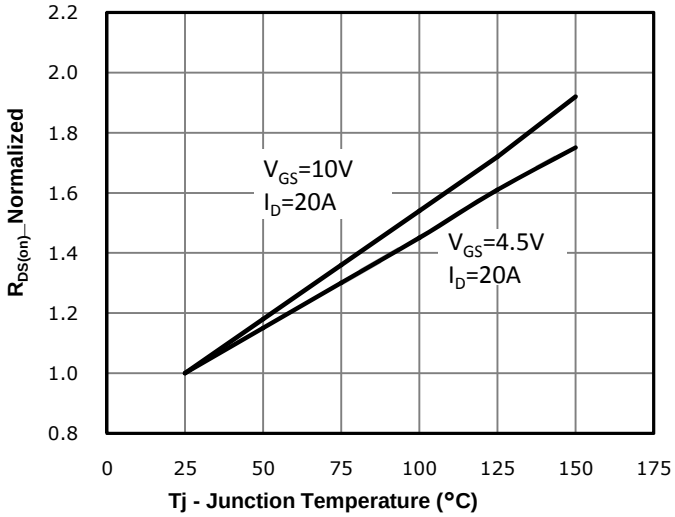


Fig 6: Capacitance Characteristics

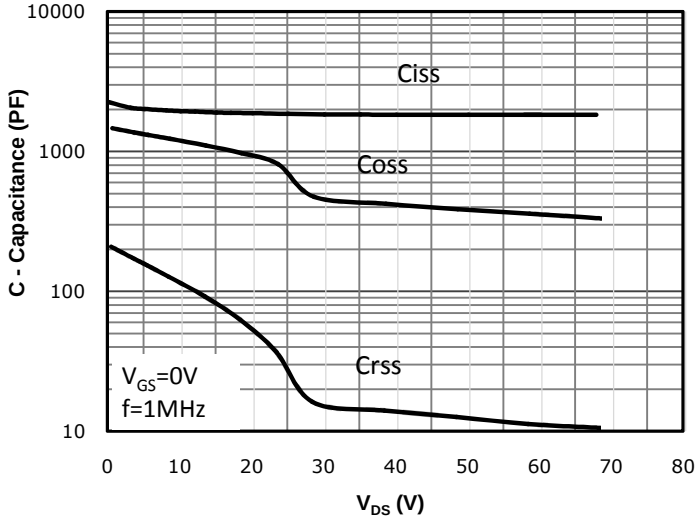


Fig 7: Gate Charge Characteristics

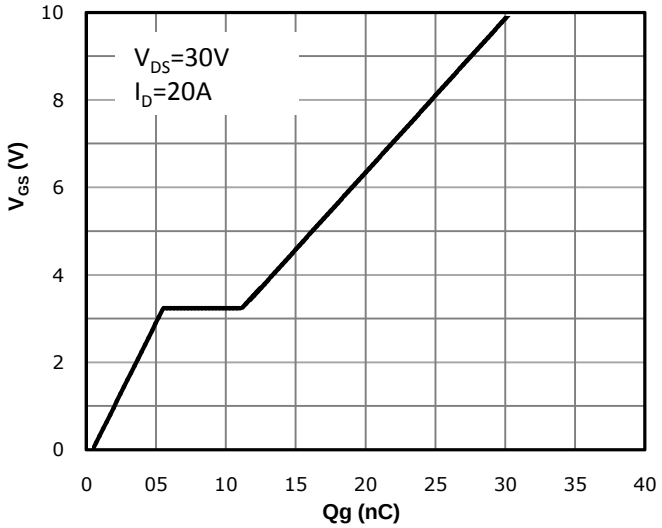


Fig 8: Body-diode Forward Characteristics

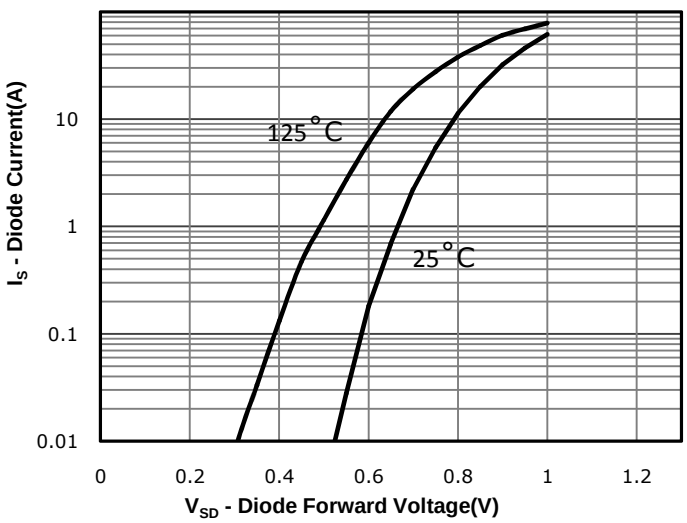


Fig 9: Power Dissipation

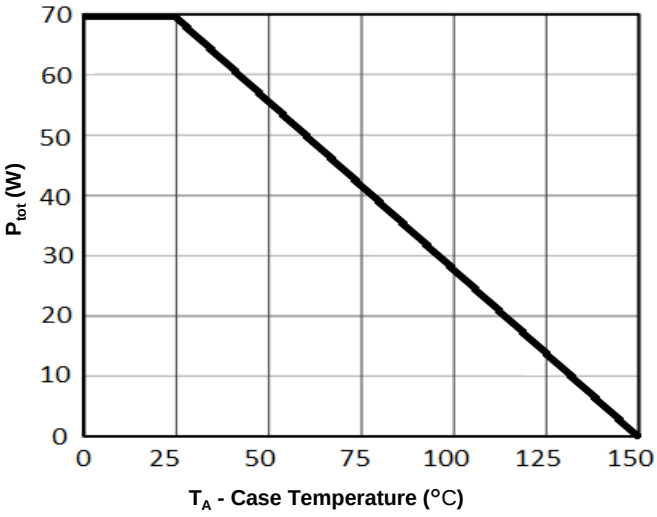


Fig 10: Drain Current Derating

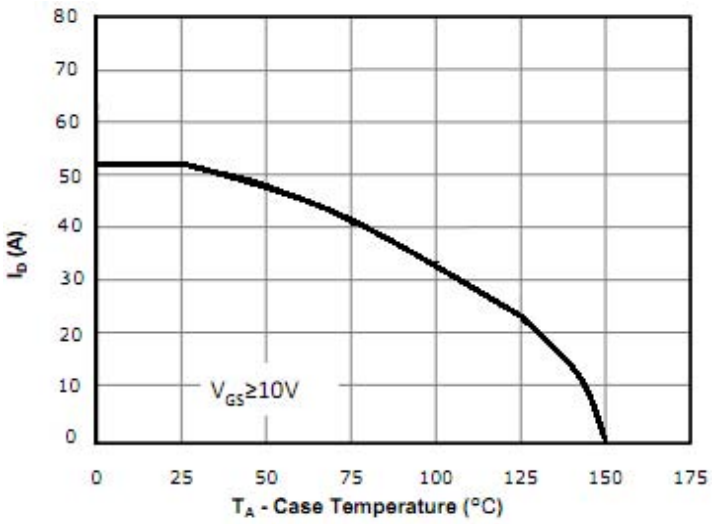


Figure A: Gate Charge Test Circuit & Waveforms

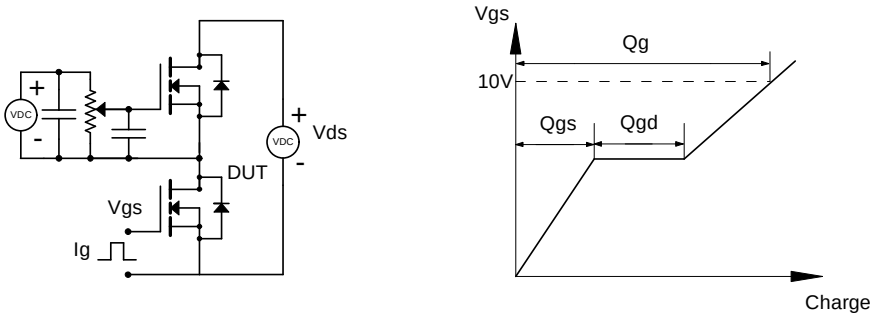


Figure B: Resistive Switching Test Circuit & Waveforms

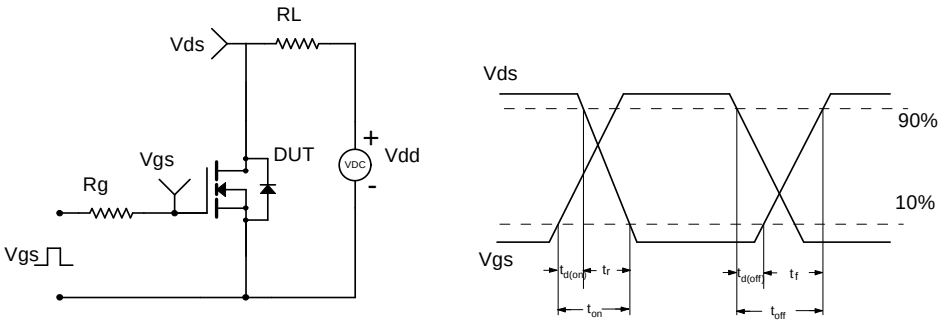


Figure C: Unclamped Inductive Switching (UIS) Test

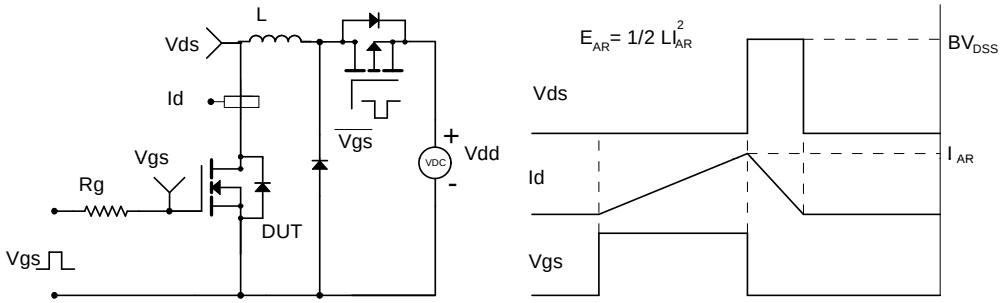
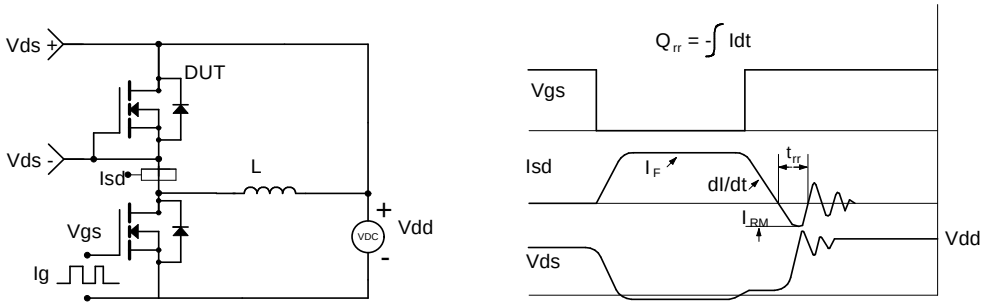
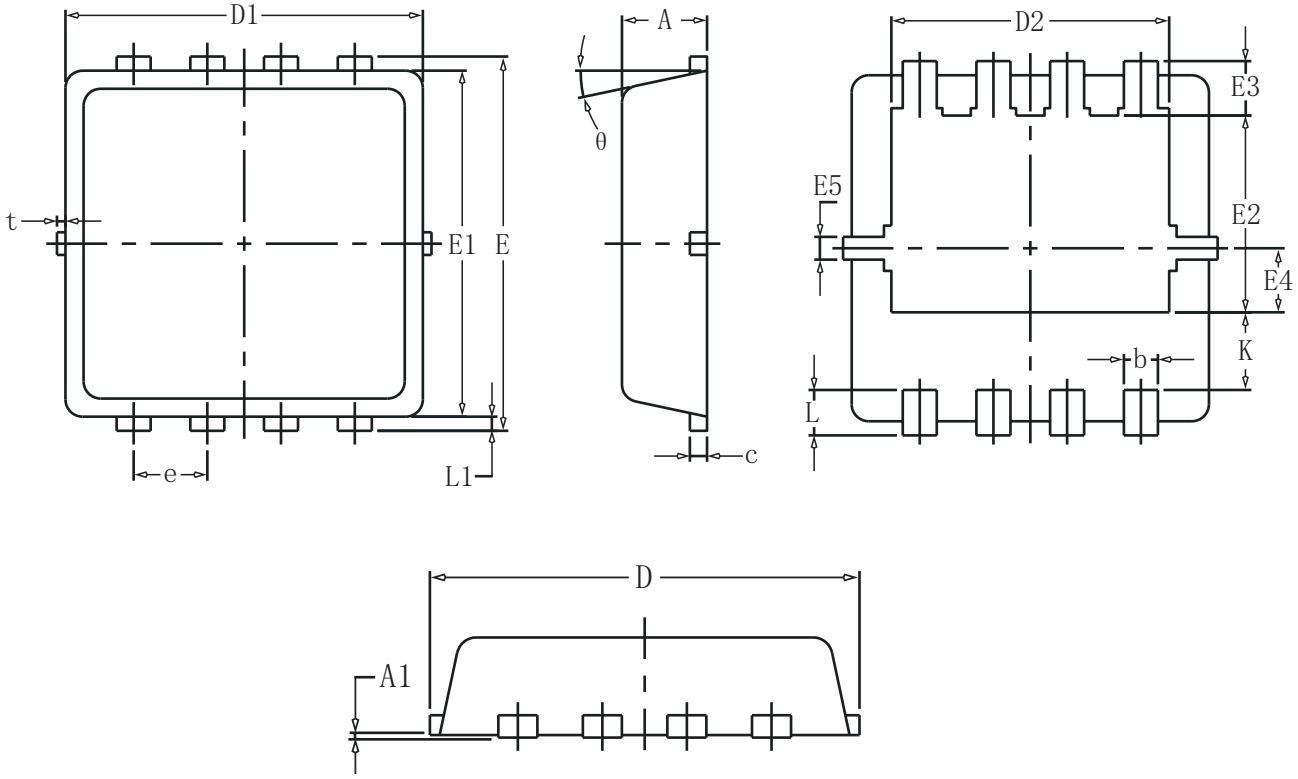


Figure D: Diode Recovery Test Circuit & Waveforms



DFN3X3-8L Package information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	–	–	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°